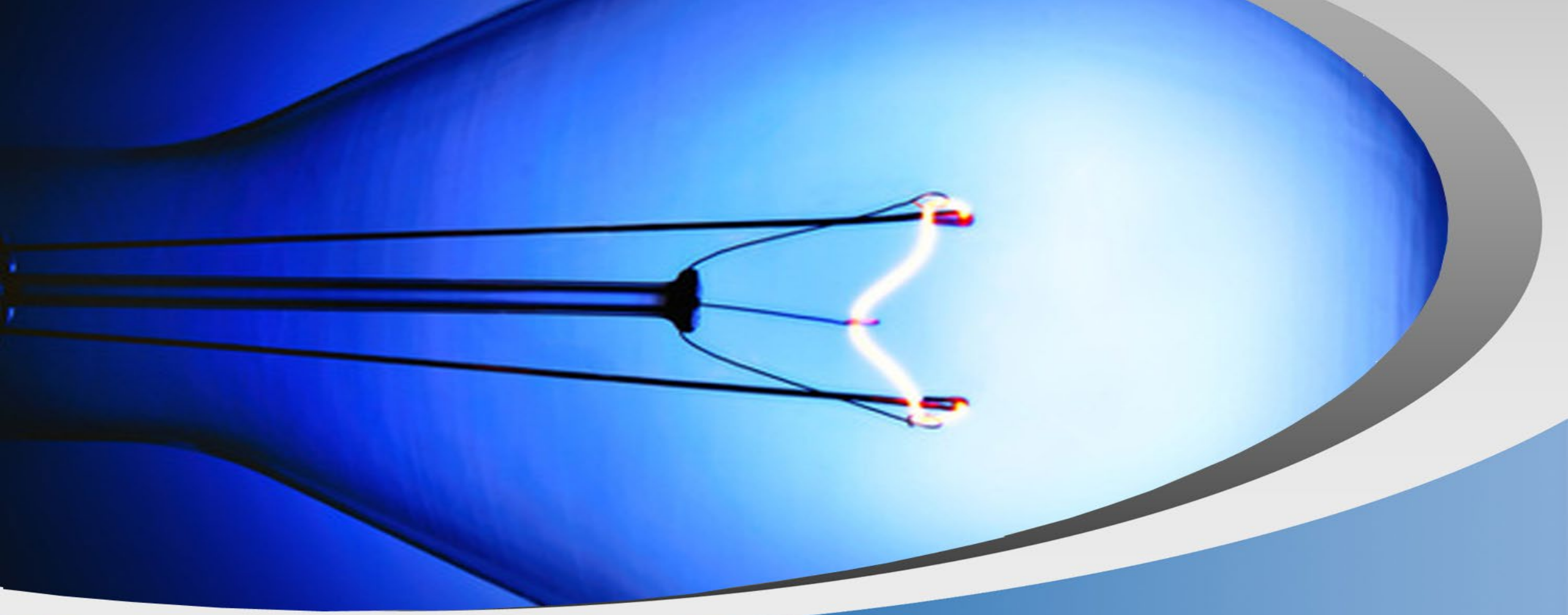

Accellera Overview 2019

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SYSTEMS INITIATIVE

Accellera Systems Initiative

Our Mission

To provide a platform in which the electronics industry can collaborate to innovate and deliver global standards that improve design and verification productivity for electronics products.

Broad Industry Support

Broad Industry Support

Associate Members

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Broad Industry Support

Start-Up and University

Benefits of Membership

- **Join Accellera to get EARLIER access to leading edge design and verification technologies – sometimes many years earlier!**
- **Become a Corporate member to drive the standardization process – influence what Accellera should work on next.**

A Proven Standards Approach

For the Systems and Semiconductor Design Community:

- Drive standardization efforts
- Ensure standards meet your needs
- EDA implementation choices

For the EDA Company:

- Compete based on innovation and implementation
- Allow development of product for general market
- Resolve integration issues at customer site to reduce cost of sales

Accellera News

- **Standards**
  - Accellera Announces Standardization Initiative to Address Design Automation and Tool Interoperability for Functional Safety – October 2019
  - Accellera Announces Proposed Working Group to Standardize UVM Analog/Mixed-Signal Extensions – April 2019
  - Accellera Formed IP Security Assurance Working Group – September 2018
  - Accellera Approved New Portable Test and Stimulus Standard – June 2018
  - Accellera Advanced the SystemC Ecosystem with a New Core Language Library and the SystemC CCI LRM – June 2018
- **Awards**
  - Tom Fitzpatrick received 2019 Accellera Technical Excellence Award for his outstanding contributions to UVM and Portable Stimulus

DVCon – Global Presence

32nd Annual DVCon U.S.

www.dvcon-us.org

4th Annual DVCon China

www.dvcon-china.org

5th Annual DVCon India

www.dvcon-india.org

6th Annual DVCon Europe

www.dvcon-europe.org

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Accellera and DVCon

- **Accellera has been successfully sponsoring "DVCon" in the US for 30+ years**
  - Original events had different names, and were tied to VHDL International and Open Verilog International
  - Eventually VHDL and Verilog focused groups merged into a single conference, and became DVCon in 2003
- **Expanded internationally in 2014: DVCon Europe, DVCon India**
  - Added DVCon China in 2016
  - DVCon India is back for 2019
- **Every DVCon has a similar "Look & Feel", with focus on user contribution**
  - Papers written by and presented by users, not just papers about products paid by sponsors
  - Panel sessions on current hot topics
  - Tutorials related to relevant standards

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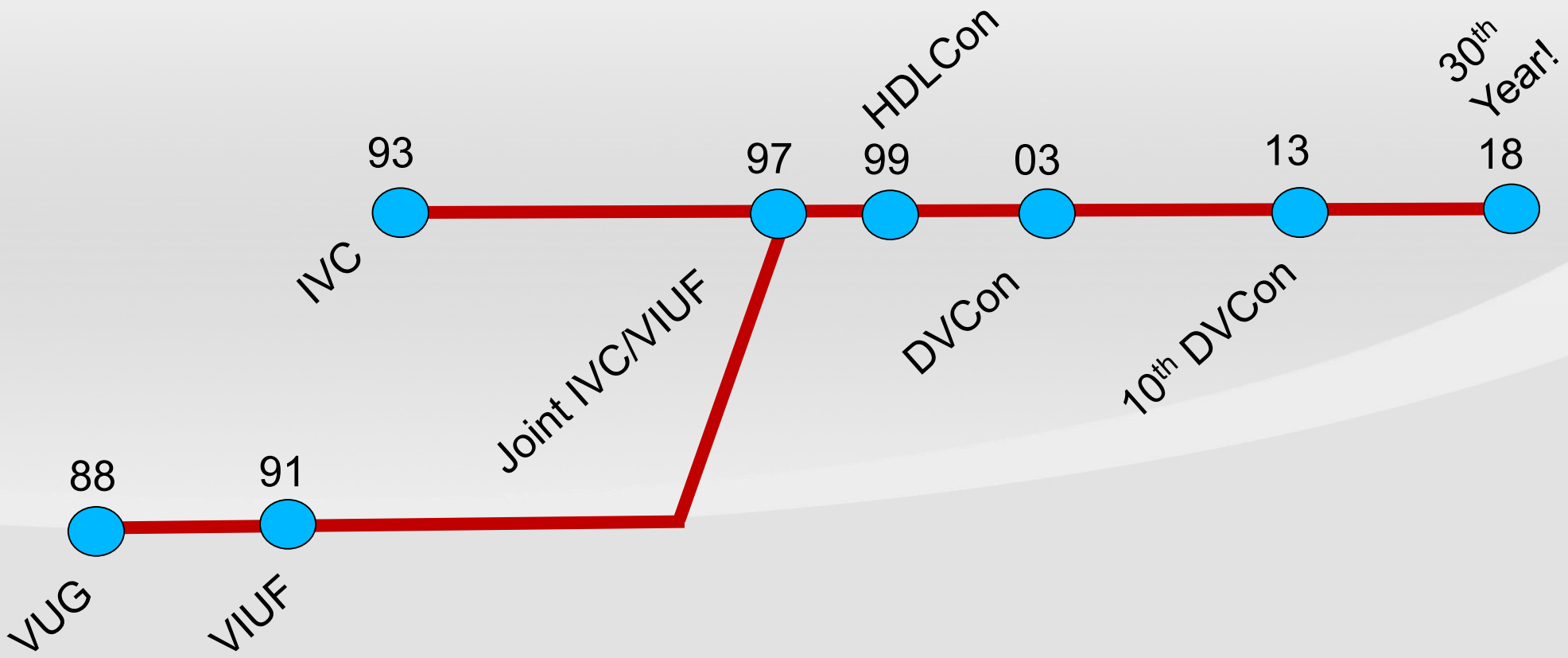
History of DVCon



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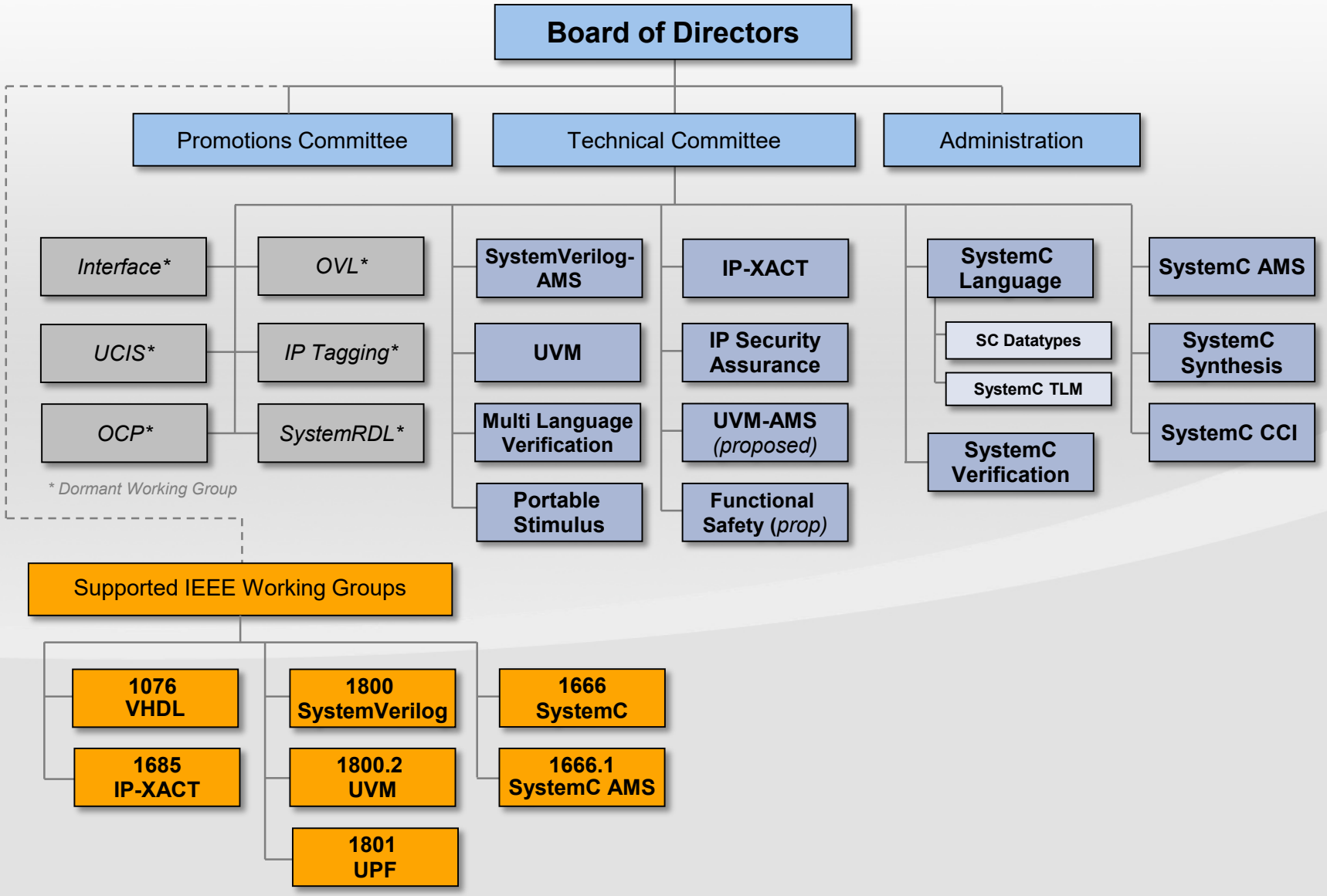
Accellera Systems Initiative



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Ongoing Technical Activities

Current Standards and Activities

- Open Verification Library (OVL) 2.8.1
- Verilog-AMS (V-AMS) 2.4
- Standard Co-Emulation Modeling Interface (SCE-MI) 2.3
- Unified Coverage Interoperability Standard (UCIS) 1.0
- IP-XACT - Update of IEEE P1685 and Vendor Extensions
- Intellectual Property (IP) Tagging 1.0
- Multi-Language (ongoing)
- Portable Stimulus 1.0a
- SystemVerilog-AMS (ongoing)
- SystemC Configuration, Control & Inspection (CCI) 1.0
- SystemC Synthesis 1.4.7
- SystemC Analog Mixed-Signal (AMS) 2.0
- SystemC Core Language and Examples 2.3.3 (includes TLM 2.0)
- SystemRDL 2.0
- Open Source Companions:
  - UVM Reference Implementation 1.2
  - SystemC Regression Test Suite 2.3.3
  - SystemC Verification Library (SCV) 2.0
  - UVM-SystemC (beta version)

Strong Partnership with IEEE

- IEEE Get program allows access to EDA & IP standards worldwide
- Download for free
  - 1666 SystemC
  - 1666.1 SystemC AMS
  - 1685 IP-XACT
  - 1800 SystemVerilog
  - 1800.2 UVM
  - 1801 UPF
- Ongoing collaboration with the IEEE Standards Association
  - 1666 SystemC Language
  - 1666.1 SystemC Analog Mixed-Signal (AMS)
  - 1685 IP-XACT
  - 1800 SystemVerilog
  - 1800.2 Universal Verification Methodology (UVM)
  - 1801 Unified Power Format (UPF)
  - 1850 Property Specification Language (PSL)

IEEE Standards Access at No Charge

- Accellera relationship with the IEEE-SA
- Accellera will release 10 standards for 10 years under an extended Get IEEE program
- More than 98,000 downloads to date!

Download IEEE Standards

http://ieeexplore.ieee.org/Xplore/home.jsp

- or find links to specific standards at -

www.accellera.org/downloads/ieee

Looking Forward

- **Functional Safety Proposed Working Group**
  - First meeting will be held December 6, 2019 in Munich
- **UVM-AMS Proposed Working Group**
  - First meeting held in Munich May 22, 2019
  - Board now considering full WG status
- **IP-XACT Working Group**
  - Working Group held face-to-face earlier this month
  - Developing a revision to IEEE P1685
  - IP-XACT release with 30+ new features targeted for mid-2021
- **Portable Stimulus Working Group**
  - PSS 1.0 Case Studies are now available
  - Released PSS 1.0a in February 2019
  - PSS 1.1 targeted for early 2020

Looking Forward

- **IPSA Working Group**
  - 43 participants from 16 companies
  - Formed 2 subgroups:
    - EDA Subgroup – focused on tools to generate collateral
    - KSC Subgroup – focused on creating knowledge base of Known Security Concerns
  - Working on proof of concept for late 2019
- **Members & Potential Members Drive Standardization Efforts into New Areas**
- **DVCon Well-established Around the Globe**
  - DVCon Europe
    - Increased European participation in working group activity
    - SystemC Evolution day is now co-located
  - DVCon China continues to grow, looking at expanding program in 2020

THANK YOU

Thank you to our Accellera Global Sponsors

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